## Claims:

A trench DMOS transistor having overvoltage protection, comprising:
a substrate of a first conductivity type;

a body region on the substrate, said body region having a second conductivity type;

at least one trench extending through the body region and the substrate; an insulating layer that lines the trench and overlies said body region; a conductive electrode in the trench overlying the insulating layer; a source region of the first conductivity type in the body region adjacent to the trench;

an undoped polysilicon layer overlying a portion of the insulating layer; and a plurality of cathode regions of the first conductivity type in the undoped polysilicon layer; and

at least one anode region in contact with adjacent ones of the plurality of cathode regions.

- 2. The transistor of claim 1 wherein said insulating layer is an oxide layer.
- 3. The transistor of claim 1 wherein said conductive electrode is polysilicon.
- 4. The transistor of claim 1 further comprising a drain electrode disposed on a bottom surface of the substrate.
- 5. The transistor of claim 4 further comprising a source electrode coupled to the source region.
- 6. The transistor of claim 2 wherein said oxide layer has a thickness between about 500 and 800 angstroms.

- 7. The transistor of claim 1 wherein said conductive electrode comprises a second layer of undoped polysilicon and a layer of doped polysilicon disposed over said second undoped polysilicon layer.
- 8. The transistor of claim 1 wherein said undoped polysilicon layer has a thickness between about 5,000-10,000 angstroms.
- 9. The transistor of claim 1 wherein said undoped polysilicon layer overlies a portion of the insulating layer vertically displaced from said at least one trench.
- 10. The transistor of claim 9 wherein said undoped polysilicon layer overlies a portion of the insulating layer that is also vertically displaced from the body region.
- 11. The transistor of claim 9 wherein said plurality of cathode regions and said at least one anode region are disposed in said portion of the insulating layer vertically displaced from said at least one trench.
- 12. The transistor of claim 1 wherein said plurality of cathode regions include boron implanted therein.
- 13. A method of making a trench DMOS transistor having overvoltage protection, said method comprising the steps of comprising:

providing a substrate of a first conductivity type;

depositing a body region on the substrate, said body region having a second conductivity type;

forming at least one trench extending through the body region and the substrate:

depositing an insulating layer that lines the trench and overlies said body region;

depositing a conductive electrode in the trench overlying the insulating layer;

implanting a dopant of the first conductivity type to form a source region in the body region adjacent to the trench;

depositing an undoped polysilicon layer overlying a portion of the insulating layer; and

implanting a dopant of the first conductivity type to form a plurality of cathode regions in the undoped polysilicon layer, said plurality of cathode regions being separated by at least one anode region.

- 14. The method of claim 13 wherein the implanting steps forming a source region and a plurality of cathode regions are performed simultaneously.
- 15. The method of claim 13 further comprising the step of defining a photolithographic mask over the body region and the undoped polysilicon layer.
- 16. The method of claim 12 wherein the step of depositing an undoped polysilicon layer is performed before the implanting step.
- 17. The method of claim 12 further comprising the step of etching the conductive electrode to expose a portion of the insulating layer overlying the body region.
- 18. The method of claim 12 further comprising the step of etching away a portion of the undoped polysilicon layer overlying the body region and said at least one trench.
- 19. The method of claim 12 wherein said insulating layer is an oxide layer.
- 20. The method of claim 12 wherein said conductive electrode is polysilicon.
- 21. The method of claim 12 further comprising the step of forming a drain electrode on a bottom surface of the substrate.

- 22. The method of claim 21 further comprising the step of forming a source electrode coupled to the source region.
- 23. The method of claim 19 wherein said oxide layer has a thickness between about 500 and 800 angstroms.
- 24. The method of claim 23 wherein said conductive electrode comprises a second layer of undoped polysilicon and a layer of doped polysilicon disposed over said second undoped polysilicon layer.
- 25. The method of claim 13 wherein further comprising the step of implanting boron into at least said plurality of cathode regions and said anode to achieve a prescribed diode breakdown voltage.